#8/a
S. Cotta
6-5-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Application of: **KATAKURA, et al.**

Group Art Unit: **2124**

Serial No.: **09/522,470**

Examiner: **Chat C. Do**

Filed: **March 9, 2000**

P.T.O. Confirmation No.: 3147

For: **LOGIC CIRCUIT**

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

June 3, 2003

Sir:

In response to the Office Action dated **January 3, 2003**, please amend the above-identified application as follows:

IN THE ABSTRACT:

Delete the current Abstract and replace therewith the attached substitute Abstract.

IN THE CLAIMS:

Please amend claims 1-2 and 7-8 as indicated below:

Please cancel claims 3-6 and 9-12.

1. **(Amended)** a logic circuit, comprising:

a first inversion section for inverting a first input signal having one of positive logic and negative logic and outputting an inverted first input signal;